New Development of X-ray Assisted Device Alteration (XADA) for Circuit Debugging: A Solution for Backside Power Delivery (BPD)

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INTRODUCTION

Backside power delivery (BPD) is widely anticipated by the semiconductor industry to be a pivotal development, enabling more efficient power delivery due to reduced resistance and significant improvements to transistor density (20-30% cell area reduction). The big three major IC manufacturers (Intel, TSMC, and Samsung) have all announced their intent to implement BPD by their next nodes.

The challenge with BPD is that existing circuit debugging / marginal fault isolation techniques such as LADA (laser assisted device alteration) will become obsolete. LADA has become a well-known standard approach, in which the silicon backside of the device is thinned such that it is transmissive to a laser (e.g. 1064nm wavelength). A tester then electrically stimulates a device and a laser generates photo carriers in the device, which can trip a passing device to a fail condition (or conversely, from a fail into a pass condition). Significant development in LADA has enabled spot sizes of 100-200nm, thus enabling it to isolate a small area of transistor cells.

Because LADA requires backside silicon thinning, the shift to BPD in which power rails are placed on the backside means this approach will no longer work. NIR is not sufficiently transmissive through silicon, let alone layers of copper power rails. Thus circuit debugging needs a dramatically new approach to address emerging BPD schemes.

One of the most promising approaches is using X-rays instead of NIR in a newly developed approach called X-ray Assisted Device Alteration (XADA). Because X-rays are sufficiently transmissive to copper and silicon, little to no sample preparation (e.g., backside thinning) is required and the intact device can be probed. However, there have been significant concerns about the viability of X-rays that have restrained the enthusiasm for its potential, including whether they are *too* transmissive (thus not interacting sufficiently with the sample) and whether they permanently alter the device [2]. Here we will present a completed XADA prototype and present results of the system, validating its usefulness for BPD devices.

SYSTEM OVERVIEW

Sigray has developed an X-ray Assisted Device Alteration tool simply named Sigray XADA™ (Fig. 1B) in partnership with Intel [1]. The system can achieve a spot size of <2.5 µm spot size with a high flux of >$2.5e^5$ ph/s/µm^2 with x-rays of operating energies between 5 to 9 keV. The system was designed using Sigray's patented x-ray component technologies of an ultrahigh brightness x-ray source and high efficiency x-ray imaging optics. To ensure the maximum flexibility of the tool, a large and flexible tester area was designed with large cable runs so that a tester can go in and out without needing to disconnect the cables. The software enables an externally supplied triggering voltage pulse to advance the stage in a rastering pattern to spatially localize the fault.

Feasibility Demonstration

Prior to the release of the Sigray XADA™, Sigray collaborated with Dr. William Lo of NVIDIA to perform baseline tests on the feasibility of X-rays for fault isolation and presented these results at ISTFA 2022 [2]. The preliminary results were performed in a Sigray AttoMap™ tool, which is an ultrahigh resolution microXRF system sold for geological, biological (metallomics), and semiconductor dopant/residue research applications (Fig. 1A). Sigray AttoMap™ uses similar critical components (Sigray x-ray source and x-ray optics) as the XADA tool, but is limited in its ability to accommodate testers and its stability/repeatability to enable moving toward submicron resolution. The results with AttoMap™ indicated a minor, but perceptible, VT shift on a 5nm FinFET test vehicle. A follow-on experiment conducted and presented by Dr. Lo at a 2023 ISTFA user group used a series of inverters and buffers in a 5nm test chip with large separations between transistors (50 µm) to ensure the x-rays were only perturbing one transistor. The pulse out of the device was compared to the input pulse to determine the delay using a high bandwidth oscilloscope. A 3-4ps timing delay was seen, with a delay persistence of >10 minutes (Fig. 2A).

This study was then followed up with an Intel collaboration. In this, a preliminary baseline test was performed to demonstrate an x-ray induced change of the switching time of a single CMOS inverter in a chain (Fig. 2B), similar to the NVIDIA study. The delay was shown to scale with x-ray exposure time linearly (Fig. 2B). This was followed by a real-world example in which the device had a known failure at a worldline-to-ground short in an SRAM cell. The device was rastered using Sigray XADA™ (Fig. 1B) at 2.4 µm step sizes over a 30 x 60 µm region and using a spot size of ~5 µm. Because x-rays produce persistent effects in datasets, the workaround solution was to use variable raster directions to successfully localize the fault (Fig. 2C) [1].

Future Directions

During our presentation, we will discuss additional developments planned for XADA, including potential roadmaps toward submicron spot sizes and additional updates on experimental validation.

FIGURE 1. Left (1A): Sigray AttoMap™ used for initial feasibility tests with Dr. William Lo (NVIDIA). Right (1B): Sigray XADA™ used for additional feasibility tests in collaboration with Intel.

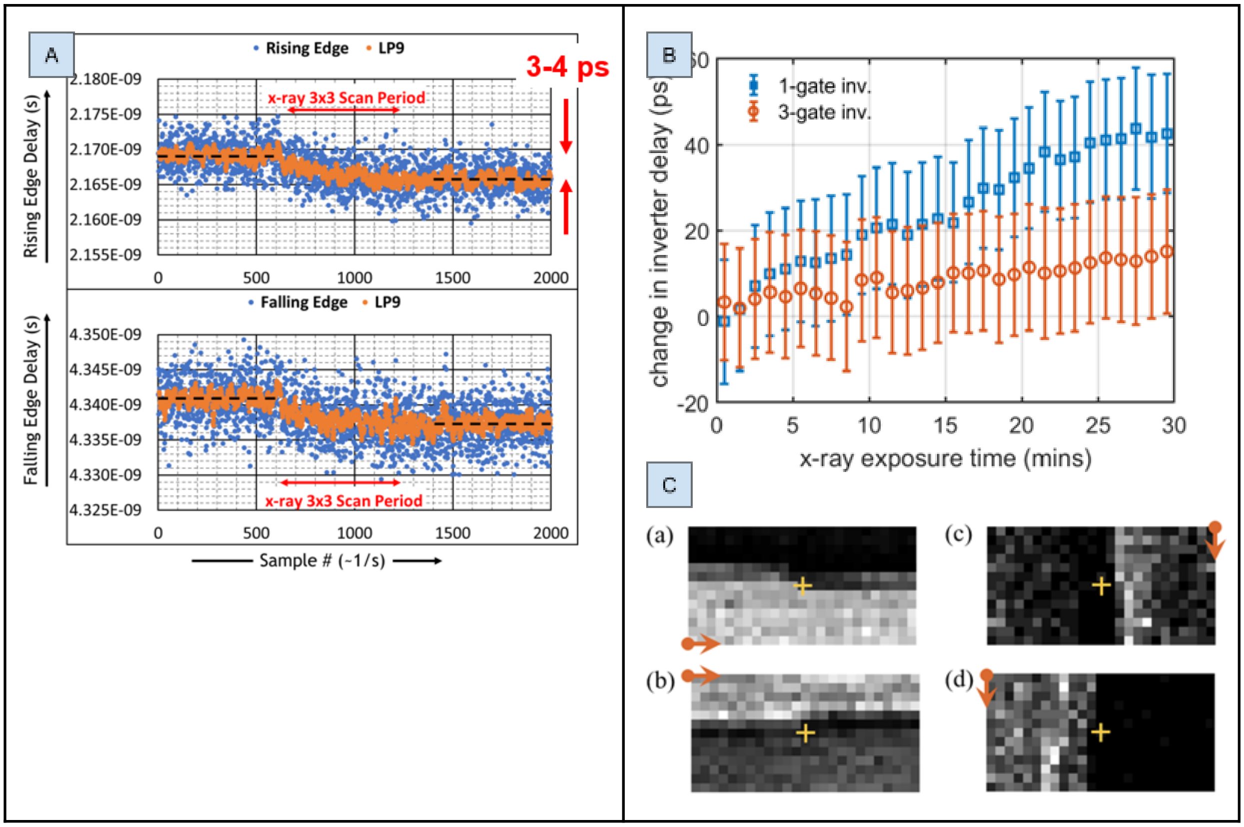

FIGURE 2. Left (2A): Results obtained with Sigray AttoMap™ on a 5nm DUT devised by Dr. Lo at NVIDIA. Right (2B): Changes in a single CMOS inverter , showing that delay scales with x-ray exposure time. Right (2C): Variable angle rastering enabled isolation of a physical defect (short) located at the yellow crosshairs. White pixels correspond to more failing tests and black pixels to fewer.

REFERENCES

1. KC Celio, et al. Laboratory X-ray Assisted Device Alteration for Fault Isolation and Post-Silicon Debug. *IRPS* (2024).
2. W Lo, et al. Device Alteration Using a Scanning X-ray Microscope. *ISTFA* (2022).

KEYWORDS

X-ray, Fault Isolation, LADA, XADA, Circuit Debugging, Laser Voltage Probing, SDL, Marginal Failure, Backside Power Delivery (BPD)